

### **CE-ATA Technical Errata**

Errata ID	Protocol 022
Affected Spec Ver.	Protocol 1.0
Corrected Spec Ver.	

#### Submission info

Name	Company	Date
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Description of the specification technical flaw (add space as needed)

The specification is ambiguous regarding whether the host is required to write the entire taskfile when using RW\_MULTIPLE\_BLOCK (CMD60) to issue an ATA command. This erratum requires that the entire taskfile be written in this case.

## Description of the correction

#### The first paragraph of section 2.1.1 shall be modified as shown:

The RW\_MULTIPLE\_REGISTER (CMD60) command allows the reading and writing of one or more registers with a single MMC command. Register accesses with this MMC command are always for an integral number of Dwords and have a Dword aligned register address. The RW\_MULTIPLE\_REGISTER (CMD60) command supports issuing an ATA command by having the complete ATA task file image transmitted in a single MMC command sequence. The entire taskfile shall be written when issuing an ATA command with RW\_MULTIPLE\_REGISTER (CMD60). Specifically, the Address shall be 0h and the Byte Count shall be 10h (16 bytes). Figure 1 depicts the RW\_MULTIPLE\_REGISTER (CMD60) command structure.

# Disposition log

1/9/2006 Erratum captured 1/11/2006 Updated section number to modify 3/12/2006 Erratum ratified
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